Claims

1. A data transfer circuit for latching an input data in a first latch section, transferring data of a latch result of said first latch section to a second latch section, and latching therein, characterized in:

transferring data of only an inverted output of the latch result of said first latch section or only a non-inverted output of said latch result to said second latch section; and

at least during a period of data transfer of the latch result of said first latch section to said second latch section, causing for a power voltage of said first latch section to rise.

2. A flat display apparatus that sequentially inputs gradation data indicative of brightness of each pixel and displays an image based on said gradation data in a predetermined display section, said flat display apparatus characterized by having:

a plurality of latch circuits for sampling said gradation data sequentially and cyclically, and distributing said gradation data to a corresponding line; and

a digital/analog conversion circuit for setting an output signal level to said corresponding line depending on a latch result of said latch circuits, in which each of said plurality of latch circuits is characterized by:

latching said gradation data in a first latch section at a respective timing corresponding thereto, data transferring a latch result of said first latch section to a second latch section simultaneously and in

parallel in said plurality of latch circuits to output the result to said digital/analog conversion circuit;

data transferring only an inverted output of the latch result of said first latch section or only a non-inverted output of the latch result of said first latch section to said second latch section; and

raising a power supply voltage of said first latch section at least during a period of data transfer of the latch result of said first latch section to said second latch section.